

REMARKS/ARGUMENTS

Introduction:

No claims are amended or added. Claims 2, 4-6, 8-16, and 37 remain pending in the application. Applicant respectfully requests reexamination and reconsideration of the application.

Objections To Drawings:

The drawings were objected to under 37 CFR 1.83(a) on grounds that the drawings allegedly do not show a plurality of sockets and an unsingulated wafer. Applicant respectfully traverses the objection. The specification describes a non-limiting example in which an unsingulated wafer, an example of which is illustrated in Figure 8A as element 802, can replace the singulated devices 702 in Figure 7. (Specification, page 26, lines 3-19.) The drawings thus illustrate a non-limiting example of a plurality of sockets (e.g., 704 in Figure 7) and a non-limiting example of an unsingulated wafer (e.g., 802 in Figure 8A), and the specification states that the sockets 704 can be used to test the wafer 802. (Specification, page 26, lines 3-19.) Applicant respectfully submits that the illustration of a plurality of sockets 704 and a wafer 802 in the drawings and the description in the specification that the sockets 704 can be used to test the wafer 802 fully meets all of the requirement of 37CFR 1.121(d). Applicant therefore requests that the objection to the drawings be withdrawn.

Rejections Based On Prior Art:

Claims 2, 4-5, 8, 14-16, and 37 were rejected under 35 USC 103(a) as unpatentable over US Patent No. 6,087,845 (Wood) in view of US Patent No. 6,087,845 (Farnworth), Gareshi and Hembree. Applicant respectfully traverses this rejection on the grounds that there is no motivation to combine the prior art as proposed by the PTO, and thus, the only way in which the PTO combined the references was through impermissible hindsight.

The PTO acknowledged that Wood's wafer 30 (which the PTO equated with "the semiconductor devices" of claim 2) does not include "a plurality of elongate, spring connection elements," as would be required to meet the recitations of claim 2. The PTO alleges, however, that it would have been obvious to replace Wood's wafer 30 with Farnworth's substrate 12, which includes spring segments 34, 38, 40 (see Farnworth Figures 3A-4B). The purpose of Farnworth's

spring segments, however, is to provide a biasing contact force in order to establish electrical connections. (See Farnworth col. 2, lines 48-50.) Wood, however, teaches away from the need for spring segments on a wafer for biasing to establish electrical connections on two accounts:

First: For the purpose of “biasing” or providing a contact force between wafer 30 and contact tips 31 Wood teaches that a separate biasing mechanism 43 of figure 3 be included in the support plate 12 (see Wood specification column 6 at 5). Claim 1 of Wood includes the limitation that “a first support member a biasing assembly located thereon,.....” Such language and description is illustrative that Wood would not look to Farnworth for contact springs to place on a wafer in order to provide a contact force. Woods biasing solution combined with the contact springs of Farnworth would create a less predictable second degree of freedom in movement and therefore would be less advantageous. There is therefore no need—and indeed no reason—for Wood’s wafer to be replaced by one of Farnworth’s type.

Second: For the purpose of overcoming irregular, non-flat wafer 30 surfaces Wood demonstrates the use of a flexible conductive substrate 63 which is “likely to conform the wafer 30” of figure 4 to aid in making electrical contact. (See Wood specification column 5 at 35.) Here again, rather than looking to a Farnworth type wafer Wood uses a more complex means for providing contact by bringing an additional element into the mechanism. Wood independent Claims 17 and 22 of Wood contain the language inclusive of another substrate 63 in order to make contact between wafer and “contact elements.” There is no reason for Wood’s wafer to be replaced by one of Farnworth’s type because of the solution presented and claimed in Wood.

For generally the reasons discussed above with respect to claim 2, the prior art does not teach or suggest replacing Wood’s wafer 30 with Farnworth’s electronic device, and in fact, Wood teaches away from the combination. Claim 2 is therefore patentable over Wood and Farnworth. Gareshi and Hembree have no bearing to claim 2 and were cited by examiner to pertain only to dependent claims 14-16.

Claims 4-5, 8, 14-16, and 37 are dependent of patentable claim 2, reciting additional features, and therefore should be patentable under the same reasoning as discussed above for claim 2.

Claims 9-13 have been rejected as being unpatentable under 35 U.S.C. 103(a) over Wood and Farthworth, Hembree, Igarashi, Pammer, Russel, and Smith. Applicant respectfully traverses this rejection. For the same reasons as claim 2 above, from which claims 9, 10, and 13

depend, claims 9, 10, and 13 are patentable. Without the combination of Wood and Farnworth upon which to add Hembree, Igarashi, Pammer, Russel, and Smith, the combination fails to approximate the invention of Applicant.

Claim 11 recites "a plurality of power lines disposed on the substrate." Claim 11 further states that "each said power line correspond[s] to one of said rows of socket substrate and suppl[ies] power to every socket substrate in said row." The apparatus of claim 11 is advantageous because it reduces the number of power lines needed to power the sockets by providing power from a single power line to all of the sockets in a row. Claim 12, which depends from claim 11, adds "isolation resistors" "disposed between one of said power lines and one of said socket substrates." The apparatus of claim 12 is advantageous because the resistors can provide a measure of electrical protection between the sockets. For example, if one socket is electrically connected to a die that has a power input pad that is shorted to ground, absent the isolation resistors, the short circuit might pull the entire power line towards ground, shorting the dies that are electrically connected to other sockets in the row (and that are fed by the same power line). The isolation resistors can reduce the likelihood that a short circuit at one socket adversely affects the other sockets in a row. None of the prior art of record teaches or suggests—or provides the advantages of—the foregoing common power lines of claim 11 or the isolation resistors of claim 12. Claims 11 and 12 are therefore further patentable over the prior art of record.

Claim 6 stands rejected Under 35 U.S.C. 103(a) as being unpatentable over Wood in View of Farnworth and Hembree, Igarashi, and Horton. Applicant respectfully traverses this rejection. For the same reasons as claim 2 above, of which claim 6 depends, claim 6 is patentable. With out the combination of Wood and Farnworth upon which to add Hembree, Igarashi, Pammer, and Horton, the combination fails to approximate the invention of Applicant.

Conclusion:

In view of the foregoing, Applicant submits that all of the claims are allowable and the application is in condition for allowance. If the Examiner believes that a discussion with Applicant's attorney would be helpful, the Examiner is invited to contact the undersigned at (801) 323-5934.

Respectfully submitted,

Date: May 22, 2006

By


N. Kenneth Burraston
Reg. No. 39,923

Kirton & McConkie
1800 Eagle Gate Tower
60 East South Temple
P.O. Box 45120
Salt Lake City, Utah 84111-1004
Telephone: (801) 323-5934
Fax: (801) 321-4893